When I was asked to speak here today on what the future holds for general purpose ATE designed to test complex systems on a chip (SoCs)…..I immediately thought of this guy. Does anyone recognize him? This is Isaac Newton who when asked why gravity worked the way it did. …..said, “Hypotheses non fingo” Can anybody here translate this Latin phrase?………… I guess there are no lawyers, doctors or priests in the audience. It means literally, “I ain’t got a clue.”

So since I had no idea what the future holds for ATE I decided to go “Back to the Future” so to speak…………and review the predictions of the past two or three decades.

Then Armed with that knowledge I hoped I could provide a credible foretelling of the future of ATE.I would now like to review 8 Past Predictions related to ATE and see how accurate they were or were not.

1 IDDQ testing is not viable and will be abandoned.
2 Functional testing will be replaced by structural testing
3 The ATE industry will adopt a standard test language.
4 The industry will embrace open architecture ATE
5 “Big Iron” testers will go the way of the dinosaur
6 EDA and ATE will work together for more efficient testing and problem resolution.
7 Testing costs will escalate dramatically with ATE costing over $20M
8 Built-In-Self-Test that is BIST will obsolete ATE

I would assume most of you have these predictions over the years.

So let’s explore the first prediction that IDDQ testing is not viable and will be abandoned. IDDQ testing tests CMOS for manufacturing faults. It measures supply current (I_{dd}) in the quiescent state looking for small leakage paths. IDDQ was thought to be the holy grail for detecting these pesky and damaging leakage paths. But when newer ICs containing tens of millions of transistors…..circuit partitioning and built in current sensors…….the IDDQ test became less workable. Additionally as processes shrink, the leakage current becomes much higher and less predictable. This makes it difficult to tell a low leakage part with a defect from a naturally ….high leakage part. Also, increasing circuit size means a single fault will have a lower percentage effect, making it harder for the test to detect.

The classic IDDQ has proven to be not very useful. It’s just not practical to track an IDDQ issue back to an offending area of the SOC.…..The SoC has many clock domains, …..purchased IP from multiple sources …..and other blocking issues that obscure the relationship between clock, circuit and current.

When power levels in MPUs got to crazy high levels it became almost impossible to detect the small leakage paths. …..However since the power levels of MPU’s are coming back down it’s becoming useful again.

One particular technique that helps is …..power gating where the entire power supply to each block can be switched off …..using a low leakage switch. …..This allows each block to be tested individually or in combination, …..This which makes the IDDQ tests more significant when compared to testing the whole chip.
For modern wireless devices in particular, it is important to understand all aspects of power consumption. The latest versions of IDDQ test technology should allow this to happen. For modern chips, IDDQ test allows dynamic max and min current testing as well as characterization of frequency and function. Power is one of the big performance factors for modem chips, so this portion of the IDDQ world is sounder than ever.

There’s also the Green movement pushing for power management techniques which require similar test techniques. So I guess one could say IDDQ testing is hanging in there and still has viable application

PREDICTION number 2 was that Functional testing will be replaced by structural testing

Functional testing determines if the logic is functioning as designed. For example if 1 is added to 1 does the logic produce a 2? Structural testing verifies the structure of the chip design and assumes that if the structure is correct then 1 + 1 should result in a 2. One problem, especially for new complex high speed SoC circuits, is the desired fault coverage cannot always achieved with structural testing alone. As a result there apparently is a growing need for a return to limited functional testing.

Dave Armstrong, director of SOC product engineering at Advantest says, “Clearly current structural test methods have not been able to adequately tackle “interface” faults. There is no other proven method, other than functional test, to confirm domain-to-domain issues.” Although structural testing seems to be good at ferreting out issues in device cores, these tests don’t seem to adequately address high-performance I/O fault detection. For example injecting and analyzing jitter in SERDES I/O still requires some amount of functional test equipment or external circuitry to provide a high quality test. This is especially true for higher GHz speeds.

Another emerging issue that is driving a functional test requirement at least initially, is the quickly emerging new standards for inter-chip communications in wireless and other hand-held systems, as well as PCs. Many of the high speed ports cannot be tested using loopback or other shortcuts. Others have elaborate protocol requirements that need to be tested at speed even when implemented on fast process technologies.

So it would seem complex testing problems, which are not adequately covered by structural testing, are driving a renewed need for functional test. In other words, I think Functional testing is having a revival.

PREDICTION number 3 The ATE industry will adopt a standard test language.

One common standard software language for all ATE products was thought to be a great idea. To this end the IEEE STD 1450-1999 was developed for a Standard Test Interface Language (STIL). STIL for digital testing was completed in 1999 and additional extensions were added through 2007. So it is essentially complete. The standard is being used by some more than others although it has provided a much needed vehicle for defining test patterns. STIL completed a core test language extension for embedded memories and BIST in 2005.

Although it targeted EDA companies like Mentor and Synopsys, it’s usage is questionable

STIL for flow and test method extensions has been a work in process for over 10 years. The ATE companies have never really supported this and, although a small working group is still active, the utility of this standard is doubtful. STIL for analog has had a rocky road. It has never been embraced by either the analog test companies, or the analog device designers. It has now been dormant for several years.

According to Tony Taylor, STIL Consultant, “Once the standards were done, it was expected that the activity would shift to a common user group to ensure the uniform usage of the standards. In the US the Standard Test Consortium, tasked to promote STIL, failed. In Japan the STARC and SSTAG efforts have been more successful.

The fact is the limited success of STIL may be due to companies not wanting to share their solutions with competitors or not wanting to spend money on something that they feel is really not needed. Obviously politics and economics Although all major ATE companies now have a way to import STIL, not much more has happened.

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Basically STIL has succumbed to competitive realities and the standard test language is dying on the vine.

**PREDICTION # 4:**
The industry will embrace open architecture ATE

The open architecture ATE is somewhat like a hardware standard. It was heavily promoted by Advantest and Intel. Open architecture required ATE manufacturers to develop a single set of hardware and software standards across the test industry, allowing instrumentation to be exchanged between ATE supplier boundaries.

But did it ever really exist?

Although there are a lot of similar instrumentation efforts being undertaken by ATE manufacturers ……they are competitors and the capabilities they integrate into their test modules are what differentiate them. Additionally there is no opportunity for companies to charge extra for this feature. It is considered an entitlement. There have been some software related efforts including STIL & STDF and some ATE manufacturers have developed a few common basic modules ………but for the most part they have never been used in multiple vendor products.

On the other hand …….ATE companies have for years been integrating into their architecture HW and SW from 3rd parties …..especially when driven by a customer demand, or …..a time to market demand. Even though the collective demand of the IC manufacturers may drive the theoretical desire for an open architecture ATE……….few semiconductor manufacturers really want to be ATE system integrators …….which they would have to become. So the concept of buying drop in tester options on the open market never really played out. I think the ATE industry has come to the basic opinion that it’s unrealistic for ONE open architecture to service the entire industry. No ATE vendor wanted to give up any, …….even a small differentiation …….or potential for differentiation……….in order to put their technology into the public domain.

On the other hand we are seeing more open architecture PC based testers. Over the last ten years the emergence of multi-core computing and high-bandwidth bus technologies such as PCI Express have make possible test platforms based on PC technologies. Software-defined modular instrumentation has grown from only a handful of products in 2000 to more than 1500 products today ……..from more than 70 different test vendors. ……..Presently these platforms are mainly used to test small pin count devices mostly analog in nature. For most ATE basically….. it comes down to simple market dynamics.

IC manufacturers want to reduce the differentiation in test products and make them a commodity in order to drive down the price. Tester companies want to provide clear differentiation …….and advantage over their competitors….. in order to keep the price up to a level where they can make reasonable margins. So what will happen to the incubation of the open architecture ATE? II do not think it will never hatch

The 5th PREDICTION has been around for a long time “Big Iron” testers will go the way of the dinosaur “Big Iron” testers are high performance digital and mixed signal testers ………costing millions of dollars …….to test complex high pin count, …….high speed devices. The reason for this continuing prediction is that the escalating costs of “Big Iron” ……………coupled with the adoption of structural testing and BIST …………was thought to force users to find other test solutions. There was also a likelihood of greater test partitioning to test high performance devices ……………therefore ATE manufacturers would be forced to develop more focused or dedicated testers.

Additionally older generation equipment could be employed to do structural testing after which …….a rack and stack test stand …….with instruments to test the high speed I/O parameters, …….would finish the testing job.

None of this has really happened in any meaningful way.

The need for “Big Iron” …….for leading edge test of the most advanced technologies is still the reality. …….The devices’ ability to drive into the external world ……..must be verified …….and internal test structures are not yet designed from this perspective. This is particularly relevant for high speed requirements, RF and analog/mixed signal circuits. On the other hand the Big Iron world is changing. ………Higher parallel test will decrease the total number of testers required.
The ATE systems market is already bifurcating with “big iron” at one end of this split. More and more chips are able to be production tested on “little iron” Little iron includes cheaper more focused tester, depreciated testers, and PC-based testers mentioned before Analog/Mixed signal circuits are being tested with built-out-self-test (BOST) which is load boards with modules specifically designed to test specific circuits. More on BOST later. This bifurcation is partially due to the progression of BIST ………and the fact that........in many applications the performance of the technology is ............so good.......... that it is rapidly building a gap between the application requirements ........and what the technology can do. What this means to “big iron” is that the number of systems is continually shrinking as a percentage of semiconductor shipments overall. More and more big iron will find that it is used only to debug or validate a new product and ship the first samples.

Soon after mass production starts….. the product …..or its immediate descendents that use the same core elements …..will be moved to low cost platforms. Over the next 10 years, as advances in BIST implementation becomes automated ........and as large semiconductor companies like Intel and Samsung build their own units t.....o prove out their most advanced products and technologies .............demand for “Big Iron” will diminish. So the reality is “Big Iron” will never die it will just fade away.

Another often heard PREDICTION is that EDA and ATE will work together for more efficient testing and problem resolution. The reality is that although most ATE companies have made attempts to cooperate, .............monetization disincentives the efforts Also loose collaboration makes it even tougher to bear fruit. Hybrid test like BOST can deliver value in mixed-signal test, but presents many challenges. ........... Credence tried to acquire the EDA pieces about a decade ago to overcome this issue. …but without much success. ATE and EDA companies working together for device debug and silicon bring-up ............delivers value........but is difficult to monetize because the number of licenses one can sell is limited. Yield improvement during volume production could also offer value …but the EDA companies have worked …..mostly alone …..not involving the ATE companies.

Actually a joint EDA/ATE product or application would be a missionary sale in a risk adverse environment. …..The associated value and pain are in different design and manufacturing silos …..and in different budgets …....hence the sales challenge is daunting To quote Fadi Maamari, Atrenta Engineering Director, “Basically EDA and ATE cooperation is a heterogeneous value proposition. …..Investment is high, ….....monetization of the efforts is difficult …..and the end customers do not want to pay for the perceived value”.

Politics and economics again. ………..So what we will see in the coming years is that ………Many will talk but few will cooperate

PREDICTION # 7 Testing costs will escalate dramatically with ATE costing over $20M a copy.

Back in 1988 SIA/Sematec projected ATE costs to stay flat at $10,000 per pin so that by the year 2002 ………a 2000 pin tester would cost $20M. It saw demands of higher speeds, ….....greater accuracy, …......more time sets ….........and increased memory ….....offsetting any gains from developments such as reduced IC pin counts. They also said test continues to be a major expense in IC development …......and the manufacturing chain with up to 35% of non-recurring engineering costs attributed to test development and test debug and with testers costing up to $6M a copy. They went on to predict that without BIST it may cost more to test a transistor than it costs to manufacture it.

Fortunately this prediction never came true.

Memory BIST quickly became a standard adopted by all designers. Although logic BIST has yet to make a mainstream impact …......structural testing using algorithmic pattern generators or ATPG …....coupled with Compression technology did. …...make an impact Structural testing has gone a long way in reducing the tester memory otherwise needed to contain very long functional patterns. Additionally strides in per-pin architecture, …...pin cards …...and other technical breakthroughs kept ATE costs from the predicted astronomical increases.

IBS Corp predicted an alarming rise in the cost of test as smaller line widths proliferated. Yokogawa believes that a totally new approach is necessary and that BIST and BOST do provide the solution to reducing test costs. In fact
.....although initially the cost for testing SoCs grew ....the overall cost of testing dropped. ...One of the reasons for this drop is the innovative ways companies like Sony developed new mass production test methodologies.

Sony developed a solution for mass production using depreciated memory testers to test high pin count SoCs in parallel. In this example there are 16 - 700 pin Digital Camera devices being tested in parallel at both wafer and final test. The wafer test time per device went from 6.3 seconds in the conventional test process to just 400ms in the low cost test process. Even though for final test this low cost test process requires double insertion ....the final test ....test time went from 15.8 seconds to 4.8 seconds.  The expensive logic tester is only needed to test a few parameters like JTAG, ....some special functional tests ....and certain IOL tests. BOST modules on the load board at both wafer and final test facilitate testing the Analog circuits like DDR, USB, ADCs and the like. A load board module also interfaces the scan patterns to the memory tester pins. The result of this innovative approach is a whopping 70% reduction in the cost of test.

In terms of test costs, to paraphrase Dan Hutcheson of VLSI Research ..............ATE costs rose steadily with the rise of the Japan semiconductor industry. That makes sense, because Japan’s rise was heavily predicated on higher quality and lower cost. But their cost advantage was wiped out in the late eighties when the Yen-to-Dollar exchange rate dropped. .......As this happened there was also a notable decline in ATE sales as a percent of semiconductor sales. They then held pretty steady in the early nineties as we saw the rise of Korea and Taiwan.

There was a spike in the late nineties that was due primarily to the rise of SOC's, which made obsolete .....most of the linear and logic tester base. But then it collapsed in late nineties, coming with the rise of China in assembly and test. Although China was a factor......... I also think advances in test methodologies with semiconductor manufacturers like Intel, Altera, Marvell and Sony, taking a more proactive .....role in testing processes and methodologies, .....has also impacted this reduction in cost of test.

But really the answer to the question about the cost of ATE rising or falling is a big...........“it depends”. The industry has already reduced the annual amount of test equipment purchases to 1% or less of gross revenue. .............This is down from closer to 4% 25 years ago. Paul Sakamoto, CEO of DFT Microsystems says that in the end, testers will never be a commodity due to lack of volume. Tester companies cannot lower the gross margin per system and make up the difference by selling higher volume........ because the need for significantly higher volume does not exist. Paul suspects ATE costs will be <0.5% on an average basis somewhere in the next 5 years. ................Dan says we are almost there now.

In spite of all these facts .......most customers will argue tester costs are increasing because .......test costs on fresh new designs are higher. The reality is that Test costs ........as a % of gross semiconductor shipments ........will continue decrease over time....... but customers will argue ........they are going through the roof.

And the last PREDICTION that Built-In-Self-Test (BIST) will obsolete ATE has been hotly debated since Vinod Argerwall LogicVision founder and promoter of BIST made it in 1996 In the early 90’s when BIST burst on the scene the conventional wisdom was that it would not only compliment ATE ...........but supplant it. The main driver for the expected widespread adoption of BIST technology was, as mentioned earlier, the fast-rising costs of ATE ........coupled with the growing complexity of integrated circuits. As I said earlier BIST was quickly adopted for testing embedded memory as the value was easily demonstrated. One key factor was that embedded memory had no direct connections to external pins. ...........Additionally embedded memories were regular arrays lending themselves to algorithmic test. ........Memory BIST was an ideal solution.

For logic testing there were many impediments to its adoption. It required additional silicon area. .....Many questioned the correctness of a pseudorandom logic test. ......It was also difficult to implement and could add weeks if not months to the design cycle. Also as mentioned earlier there was also the continued development and enhancement of a competing technology ATPG. ATPG was much easier to implement and with the innovated ATPG compression algorithms ......it kept ATPG abreast of the shrinking geometries. As a result, although BIST was a better solution, ......compression was adequate to get the job done. The question is how long can it keep up with the advances in semiconductor technology advancements? ........

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In the not too distant future, even the most advanced tester with compression may not be adequate for the fastest chip. ………a situation where BIST is not only the better solution ………but the only solution. It is now common to see complex devices that have functionally diverse blocks ……….built on different and mixed technologies. ………Such complex devices require high-end mixed-signal testers that possess special digital and analog testing capabilities. Analog BIST can perform these special tests with additional on-chip test circuits. ……….This will eliminate the need to acquire high-end testers. But unfortunately Analog BIST has been even slower………..than logic BIST to develop………..let alone be adopted.

Still BIST proponents are optimistic that BIST will someday be the preferred mode of testing. ……….instead of being merely an alternative to external ATE testing as it is today. As you might expect politics also plays a role in BIST adoption. Impediments to BIST adoption are often organizational, not technological. Many companies face significant internal challenges in adopting BIST.

Design feels they get little value from BIST. ……….They are driven to meet certain tape out dates, ………..BIST specifically Logic and analog BIST ………..are often seen as a necessary evil – and worse yet ………..one that may delay their tape out. These pre Madonna’s also see test in general as no value added. ………..After all their designs are perfect. On the other hand, the poor test people are begging for BIST. They need BIST to meet their objectives – to reduce the cost of test and testers But they are stuck with solving the problem on their own when the designers throw their designs over that wall between design and test. Solving this dilemma will require cross-department planning, ……….budget sharing ……….and better interdepartmental communications… as well as cooperation. The wall between design and test must be torn down. This will require skilled leadership and broad thinking by management. Some companies like Intel, Broadcom and NEC, among others, ………..recognize this reality and are seriously adopting BIST as their mainstream test strategy.

So looking into the future BIST will obsolete ATE but only when the device can completely and totally test itself. ……..memory, logic, analog and high speed I/O. Another words it will require a revolution in test. So what will constitute this revolution?

I would like to use the automobile industry as an analogy. The horse was the common mode of transportation for millennia. It got us from point A to point B……..It was literally the workhorse, no pun intended, of the transportation industry. Then along came the Model T. It was capable of being mass produced for the masses. This was not an innovation on a horse even if it was rated in horse power. It was a revolution in transportation. It led to all kinds of changes from paved roads and gasoline stations to people no longer having to shovel horse manure. Today we have rather advanced automobiles but no revolution. The new cars are bigger, more powerful, faster, more comfortable but…. they are evolutionary not revolutionary They are essentially the same as the Model T. They have a steering wheel, motor, gas pedal, and gears. They need gasoline to power them and a human to drive them. For a revolution in the automobile industry you would need an all electric car that literally drives itself; ………….that will be a revolution.

To this end I give you The Tesla Google. The all electric car that needs no driver. It is coming. ……..Tesla has a commercial electric car ………….and Google already has over a thousand miles in Silicon Valley on their self-driving car. ………….a car that does not require a human driver. Think about it……….with the Tesla Google your 10 year old kid can take it to school. Your 90 year old blind grandma can take it to the doctors. No gas stations………..Less pollution. ………..No driver licenses. No DUs. ……….Drunken driving will be a thing of the past. Highway deaths will drop by orders of magnitude. The Tesla Google would truly be a revolutionary product. And it is coming. If not in our lifetimes than certainly in our grandkids life time.

Now let’s compare this coming revolution in the automobile industry to the coming revolution in the ATE industry. When I started my career in 1962 at RCA Defense Products in Cambridge Ohio…………..I was hired to test transistors for the WS133 Minute Man missile project. ……………I used a rack and stack setup similar to this to do all the testing manually. Then in the late 60’s Fairchild Test Systems developed the Model 4000 IC tester…………..It was a revolution in testing for the semiconductor masses. ……………It was the first commercially available automatic IC tester.

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It was programmable, could test multiple parameters, it had high throughput and facilitated low cost mass production of ICs in the semiconductor industry. This was a revolution in test and the beginning of the ATE industry. Today we have very advanced testers like the Verigy PinScale tester. But it is fundamentally the same as the Model 4000. Someone has to program it. It provides stimulus to the device under test and records the response to be interpreted by a human. There are many innovations here but it is really just a Model 4000 on steroids. Revolution will only come when ATE is built into the chip and the chip can truly test itself just like the TeslaGoogle drives itself.

To this end I give you the TesterGoogle. On chip ATE. With the TesterGoogle once the wafer or packaged device, if we even have packages then, comes off the assembly line you simply Google the chip and ask it to report its status. You know like, “How are you feeling?” And the chip may respond by saying, “Well my PLL is a little erratic so I am adjusting the voltage to stabilize it. But the real problem is I am dropping some bits in my cache memory... So I just sent the nanorobot is on a mission to fix it. I expect to meet all specifications by noon and stand ready to drive that Tesla Google. Now that is revolutionary.

Just think with the TesterGoogle there will be IEEE standards for IP development. EDA will automatically add test circuits to the design. BIST tools will understand the circuits at the topological and layout levels to test for and correct faults based on models. BIST will be fully integrated into the overall EDA flow. This will have the least impact on chip area and have the greatest ease of use to the chip designer. BIST will be inserted automatically into individual cores. The high-Level EDA environment will be based on the Hierarchical Distributed BIST (HD-BIST). HD BIST will solve BIST scheduling issues in system-on-chip applications. Timing closure will be simulated and automated early in the design and manufacturing process. Design for manufacturing will include repair components like Nanorobots to repair faulty circuits.

Crazy?? Farfetched?? Do not bet on it. It is coming. So in closing I would like to make one prediction. The day that the TeslaGoogle is mainstream semiconductor devices, due to the revolutionary TesterGoogle BIST technology, will be testing themselves and ATE will finally have gone the way of the dinosaur. The 1996 prediction of Dr. Vinod Agerwal, will finally be a realized. But I would not run out and sell my ATE stock just yet.

Thank you.

Contributors to this presentation include:

- Dan Hutcheson, VLSI Research
- Tony Taylor, STIL
- Paul Sakamoto, DFT Microsystems
- Dave Armstrong, Advantest
- Mark Allison, Verigy
- Fadi Maamari, Atrenta