

Call for Papers

Silicon Valley Test Conference

San Jose - November 8-9, 2010

The new Silicon Valley Test Conference is dedicated to electronic test of devices and boards.

Test professionals are invited to submit an abstract for one or more of the Conference focus topics shown at right.

The abstract (50+ words) should be sent by e-mail not later than May 18 to svtc.abstracts@gmail.com.

We will notify the author(s) of acceptance or rejection within 30 days. The final manuscript is due by October 15.

FOCUS TOPICS

Test and design for manufacturability	Design verification and validation
Yield analysis and optimization	Interface hardware and simulation
Low-cost test	Adaptive test
High-speed I/O and RF test	Defect-based testing
Probe card design and innovation	Power issues in test
	Iddq and current test
	Loadboard and socket issues